Prompt and favorable examination on the merits is respectfully requested.

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Appendix A. Identification of Amended Material

Please amend claims 1-11 and 15-20 as follows:

1. (Amended) A device adapted to function as an antifuse, said device comprising: a first conductor[,]; a second conductor[,]; wherein the first conductor is positioned above the second conductor; and an insulator disposed between said first and second conductors, [said device having first discrete regions having a first programming voltage and second discrete regions having a second programming voltage less than said first programming voltage] wherein the first conductor has an intersection perimeter that comprises edges portions of the first conductor, wherein the edges portions of the first conductor are positioned directly above the second conductor, wherein a minimum voltage between the first and second conductors is required to create a current path between the first and second conductors through the insulator layer, and wherein the current path created by a voltage that is not less than the minimum voltage is more likely to traverse the insulator layer essentially at the intersection perimeter than elsewhere.

2. (Amended) The [invention] device of claim 1, wherein [said second discrete regions are increased in area by providing at least one of said conductors with a plurality of fingers separated by a plurality of gaps, said second discrete regions comprising at least a portion of an edge of said fingers] the insulator layer is thinner directly beneath the edge perimeter than elsewhere beneath the first conductor.

3. (Amended) The [invention] device of claim 1, wherein [said] the first conductor comprises a gate material [and said], wherein the second conductor comprises a doped [area bounded by

shallow trench isolation] region, and wherein the doped region is more highly doped directly beneath the edge perimeter than elsewhere beneath the first conductor.

4. (Amended) The [invention] device of claim 1, wherein [said first conductor is substantially orthogonal to said second conductor] the minimum voltage is equal to about a burn-in voltage for reliability testing of the device, and wherein the burn-in voltage exceeds a normal operating voltage for the device.

5. (Amended) The [invention] device of claim [4] 1, wherein [each of said plurality of fingers have a finger width, and wherein said second discrete regions are increased in area by decreasing said finger width and by forming an increased number of said fingers on said at least one conductor] the current path is oriented essentially perpendicular to both the first and second conductors.

6. (Amended) The [invention] device of claim 1, wherein [a programming event comprises a substantially vertical current path between said first conductor and said second conductor] the first conductor comprises a first plurality of fingers, wherein the fingers of each pair adjacent fingers of the first plurality of fingers are separated by a gap, wherein the fingers of the first plurality of fingers are each oriented in a first direction, and wherein the intersection perimeter comprises line segments coinciding with edge portions of the first plurality of fingers, and wherein the line segments are each oriented in essentially the first direction.

7. (Amended) The [invention] device of claim 6, wherein [said programming event comprises the application of a voltage between said first conductor and said second conductor, said voltage substantially equal to the minimum voltage sufficient to create said current path] the gap between adjacent fingers of the first plurality of fingers exposes a portion of said second conductor.

8. (Amended) The [invention] device of claim [7] 6, wherein [said minimum voltage is substantially equal to a burn-in voltage for said device] each finger of the first plurality of fingers has essentially a same width in a second direction that is essentially perpendicular to the first direction.

9. (Amended) [An antifuse on a chip comprising a dielectric material positioned between a conductor and an active area, said dielectric material having a first thickness, wherein discrete portions of said dielectric material have a second thickness less than said first thickness where an edge portion of one of said conductor and said active area overlaps the other of said conductor and said active area] The device of claim 6, wherein the second conductor comprises a second plurality of fingers, wherein the fingers of each pair adjacent fingers of the second plurality of fingers are separated by a gap, wherein the fingers of the second plurality of fingers are each oriented in a second direction, and wherein the second direction is essentially perpendicular to the first direction.

10. (Amended) The [invention] device of claim [9] 1, wherein [one of said conductor and said active area comprise a plurality of fingers having a width substantially equal to a minimum feature

size] the second conductor comprises a plurality of fingers, wherein the fingers of each pair adjacent fingers of the plurality of fingers are separated by a gap, wherein the intersection perimeter comprises line segments oriented in a first direction, wherein the fingers of the plurality of fingers are each oriented in a second direction that is essentially perpendicular to the first direction.

11. (Amended) The [invention] device of claim 10, wherein [said plurality of fingers are formed in said conductor, said fingers overlying a first portion of said active area, spaces between said plurality of fingers exposing a second portion of said active area, said first portion of said active area comprising a non-highly doped region and said second portion of said active area comprising a highly-doped region] a first finger of the plurality of fingers has a first width in the first direction, wherein a second finger of the plurality of fingers has a second width in the first direction, and wherein the second width is unequal to the first width.

15. (Amended) A method for increasing the statistical programming of an antifuse, said method comprising the steps of:

forming a first conductor and a second conductor separated by a dielectric [material] layer, wherein the first conductor is positioned above the second conductor, wherein the first conductor has an intersection perimeter that comprises edges portions of the first conductor wherein the edges portions of the first conductor are positioned directly above the second conductor, wherein a minimum voltage between the first and second conductors is required to create a current path between the first and second conductors through the dielectric layer; and

increasing [an] the length of the intersection perimeter [of said antifuse].

16. (Amended) The method of claim 15, wherein said step of increasing [an] the length of the intersection perimeter [of said antifuse] comprises the step of forming a plurality of fingers in at least one of said first and second conductors by patterning and etching, [said fingers] and wherein the fingers of each pair adjacent fingers of the plurality of fingers are separated by a [plurality of] gap[s].

17. (Amended) The method of claim 16, [wherein said step of forming a plurality of fingers comprises forming a plurality of regions of thin perimeter oxide] further comprising doping the second conductor to form a doped region in the first conductor, wherein the doped region is more highly doped directly beneath the edge perimeter than elsewhere beneath the first conductor.

18. (Amended) The method of claim 15, further comprising the step of [decreasing post-program resistance of said antifuse] applying a programming voltage not less than the minimum voltage to create the current path between the first and second conductors through the dielectric layer, wherein the current path created by the programming voltage is more likely to traverse the dielectric layer essentially at the intersection perimeter than elsewhere.

19. (Amended) The method of claim 18, wherein [said step of decreasing post-program resistance comprises the step of increasing the conductivity of portions of at least one of said first conductor and said second conductor that form a current path when said antifuse is programmed] the

dielectric layer is thinner directly beneath the edge perimeter than elsewhere beneath the first conductor.

20. (Amended) The method of claim 16, wherein [said plurality of fingers are patterned using a process selected from the group consisting of edge printing, printing with dual tone resist, and sidewall image transfer] the step of forming a plurality of fingers comprises forming a first plurality of fingers integrally with the first conductor, wherein the fingers of each pair adjacent fingers of the first plurality of fingers are separated by a gap, wherein the fingers of the first plurality of fingers are each oriented in a first direction, and wherein the intersection perimeter comprises line segments coinciding with edge portions of the first plurality of fingers, and wherein the line segments are each oriented in essentially the first direction.